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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/002,971	10/26/2001	Blaine D. Gaither	10018224-1	3480

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EXAMINER	
TSAI, HENRY	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 06/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/002,971	GAITHER ET AL.	
	Examiner	Art Unit	
	Henry W.H. Tsai	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *4/6/05*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Appeal Brief

1. In view of the Appeal Brief filed on 4/6/05, PROSECUTION IS HEREBY REOPENED. The Office Action with the new ground(s) of rejection is set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) request reinstatement of the appeal.

If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2).

Claim Objections

2. Claim 7 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject

claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form.

In claim 7, lines 2-4, it is not clear why encoding is a further step of the decoding as motioned in claim 6 since there must be an encoding first then a decoding. It is suggested to either cancellilng the claim or rearranging the claims.

Claim Rejections - 35 USC § 112

3. Claim 1-15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, line 5-6, it is not clear that when only one condition is assessed, how the other condition can be used as a basis for processing the memory since it has not be assessed. Similar problems exist in claim 14, lines 4-6.

Applicant is required to review the claims and correct all language which does not comply with 35 U.S.C. § 112, second paragraph.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Strongin et al. (U.S. Patent No. 6,645,860) (hereafter referred to as Strongin et al.'860).

Referring to claim 1, Strongin et al.'860 discloses, as claimed, a method for processing a memory access request within processing architecture, comprising the steps of: determining whether the memory access request is speculative or not based upon a first identifier (see Fig. 6A, the bit field "is the access speculative ?" in tags 502, and see also Col. 13, lines 58-62); assessing one or both of interconnect (see Col. 10, line 67 to Col. 11, lines 1-5, regarding only one memory access may be resident on PCI bus 118 at any particular time. Therefore, Strongin et al.'860's system assesses the bus interconnect such

as traffic condition in order to determine its availability) and target resource (the system memory 130 see Fig. 1) conditions in the event that the memory access request (the memory access request sent from Northbridge 104 see Fig. 1) is speculative (Note in Strongin et al.'860's system, the condition of system memory 130 certainly is assessed (or checked) such as the availability for access no matter what the memory access request is speculative or not); and either processing the request (the memory access request sent from Northbridge 104 see Fig. 1), or not (see Col. 23, lines 57-6, regarding speculative buffer checking and control logic 1102 removing the data from speculative cycle response buffer which saves the data associated with the speculative memory access request see Col. 25, lines 60-63), as a function of the conditions (note as set forth above, in Strongin et al.'860's system certainly bases on the condition of system memory 130 such as the availability for access; and the condition of bus interconnect (see Col. 10, line 67 to Col. 11, lines 1-5, regarding only one memory access may be resident on PCI bus 118 at any particular time) for processing the memory access request).

Referring to claim 14, Strongin et al.'860 discloses, as claimed, in CPU architecture (101, see Fig. 1) that initiates both speculative and non-speculative memory access requests (the

memory access request sent from Northbridge 104 see Fig. 1), an improvement comprising decode logic for determining whether the memory access requests are speculative (decoding the bit field encoded in, see Fig. 6A, "is the access speculative ?" in tags 502, and see also Col. 13, lines 58-62), and assessment logic for determining one or both of interconnect (see Col. 10, line 67 to Col. 11, lines 1-5, regarding only one memory access may be resident on PCI bus 118 at any particular time. Therefore, Strongin et al.'860's system assesses the bus interconnect such as traffic condition in order to determine its availability) and target resource (the system memory 130 see Fig. 1) conditions, the CPU architecture (101, see Fig. 1) processing speculative requests, or not (see Col. 23, lines 57-6, regarding speculative buffer checking and control logic 1102 removing the data from speculative cycle response buffer which saves the data associated with the speculative memory access request see Col. 25, lines 60-63), as a function of the conditions (note as set forth above, in Strongin et al.'860's system certainly bases on the condition of system memory 130 such as the availability for access; and the condition of bus interconnect (see Col. 10, line 67 to Col. 11, lines 1-5, regarding only one memory access may be resident on PCI bus 118 at any particular time) for processing the memory access request).

Referring to claim 16, Strongin et al.'860 discloses, as claimed, a system (101, see Fig. 1) for processing speculative memory access requests within a processing architecture, comprising: one or more requests having a bit field (see Fig. 6A, the bit field "is the access speculative ?" in tags 502, and see also Col. 13, lines 58-62) defining the requests as speculative or non-speculative; decode logic (existing inside the processor 101, se Fig. 1) for decoding the bit field to determine whether one or more memory access requests are speculative; and processing logic (existing inside the processor 101, se Fig. 1) for processing speculative memory access requests, or not (see Col. 23, lines 57-6, regarding speculative buffer checking and control logic 1102 removing the data from speculative cycle response buffer which saves the data associated with the speculative memory access request see Col. 25, lines 60-63), based on at least one of interconnect (see Col. 10, line 67 to Col. 11, lines 1-5, regarding only one memory access may be resident on PCI bus 118 at any particular time. Therefore, Strongin et al.'860's system assesses the bus interconnect such as traffic condition in order to determine its availability) and target resource (the system memory 130 see Fig. 1) conditions (note as set forth above, in Strongin et al.'860's system certainly bases on the condition of system

memory 130 such as the availability for access; and the condition of bus interconnect (see Col. 10, line 67 to Col. 11, lines 1-5, regarding only one memory access may be resident on PCI bus 118 at any particular time) for processing the memory access request).

As to claim 2, Strongin et al.'860 also discloses the step of determining whether the request is speculative comprises decoding first identifier as a first bit field (as set forth, see Fig. 6A, the bit field "is the access speculative ?" in tags 502, see also Col. 13, lines 58-62) within the memory access request.

As to claim 3, Strongin et al.'860 also discloses encoding the first bit field (as set forth, a bit field encoded in, see Fig. 6A, the bit field "is the access speculative ?" of tags 502, see also Col. 13, lines 58-62) within the memory access request to define a speculative ID of the memory access request.

As to claim 4, Strongin et al.'860 also discloses the memory access request comprising one (the memory access request sent from Northbridge 104 see Fig. 1) of an instruction, message and operational request (the memory access request sent from Northbridge 104 see Fig. 1).

As to claim 5, Strongin et al.'860 also discloses the step of determining a priority (see Fig. 6A, the bit field "Urgency

of Transaction?" in tags 502, and see also Col. 13, lines 60-62 regarding the priority of the information related to the urgency of the a transaction) of the memory access request based upon a second identifier (see Fig. 6A, the bit field "Urgency of Transaction?" in tags 502), in the event that the memory access request is speculative, and wherein the step of processing the request comprises processing the memory access request (the memory access request sent from Northbridge 104 see Fig. 1), or not, based upon the conditions (note as set forth above, in Strongin et al.'860's system certainly bases on the condition of system memory 130 such as the availability for access; and the condition of bus interconnect (see Col. 10, line 67 to Col. 11, lines 1-5, regarding only one memory access may be resident on PCI bus 118 at any particular time) for processing the memory access request) and the priority (see Fig. 6A, the bit field "Urgency of Transaction?" in tags 502, and see also Col. 13, lines 60-62 regarding the priority of the information related to the urgency of the a transaction).

As to claim 6, Strongin et al.'860 also discloses the step of determining a priority comprises decoding the second identifier (see Fig. 6A, the bit field "Urgency of Transaction?" in tags 502) as a second bit field within the memory access

request (the memory access request sent from Northbridge 104 see Fig. 1).

As to claim 7, Strongin et al.'860 also discloses comprising encoding the second bit field (see Fig. 6A, the bit field "Urgency of Transaction?" in tags 502) within the memory access request to define a priority of the memory access request.

As to claims 8, and 18, Strongin et al.'860 also discloses the memory access request (the memory access request sent from Northbridge 104 see Fig. 1) comprises one of a memory read request (see Col. 23, line 49, regarding "read" request) and a memory load request (see Col. 23, line 55, regarding "write" request).

As to claims 9, and 17, Strongin et al.'860 also discloses the step of determining comprises utilizing one of a CPU (CPU 109, see Fig. 3), chipset and memory controller (the memory controller 200, see Fig. 3) to determine whether the memory access request (the memory access request sent from Northbridge 104 see Fig. 1) is speculative.

As to claim 10, Strongin et al.'860 also discloses at least one of the CPU (CPU 109, see Fig. 3), chipset and memory controller (the memory controller 200, see Fig. 3) independently controls the step of processing the memory access request (the

memory access request sent from Northbridge 104 see Fig. 1) based on the conditions.

As to claim 11, Strongin et al.'860 also discloses the step of assessing target resource conditions comprises assessing one or more of memory utilization, memory congestion (since the requests to be processed are the memory access requests for the system memory 130 sent from Northbridge 104 see Fig. 1), buffer space utilization (the utilization of speculative cycle response buffer 1004, see Col. 23, line 53-60), and bus congestion (see Col. 10, line 67 to Col. 11, lines 1-5, since only one memory access may be resident on PCI bus 118 at any particular time. Therefore, Strongin et al.'860's system assesses the bus interconnect such as bus congestion in order to determine its availability).

As to claim 12, Strongin et al.'860 also discloses the step of assessing interconnect conditions comprises assessing one or more of bus utilization, bus congestion (see Col. 10, line 67 to Col. 11, lines 1-5, since only one memory access may be resident on PCI bus 118 at any particular time. Therefore, Strongin et al.'860's system assesses the bus interconnect such as bus congestion and bus utilization in order to determine its availability), crossbar utilization, cross bar congestion, and point to point link utilization.

As to claim 13, Strongin et al.'860 also discloses comprising the step of notifying one or more logic devices (centralized state machine 1800, see Col. 23, lines 57-60) when the memory access request is not processed (such as the data are remove from speculative cycle response buffer 1004, see Col. 23, lines 57-60).

As to claim 15, Strongin et al.'860 also discloses a prefetch unit (existing inside the processor 101, see Fig. 1) for prefetching speculative requests (the memory access request sent from Northbridge 104 see Fig. 1), wherein the decode logic detects (by detecting the bit field encoded in, see Fig. 6A, "is the access speculative ?" in tags 502, and see also Col. 13, lines 58-62) whether prefetched requests are speculative.

As to claim 19, Neufeld'901 also discloses a bus controller (Northbridge 104 see Fig. 1) for assessing one or more of bus congestion and bus utilization conditions (in the buses 115, 102, and 118 see Fig. 1).

Response to Arguments

6. Applicant's arguments mailed 4/6/05 have been considered but are moot in view of the new ground(s) of rejection. As set

forth in the art rejections above, Strongin et al.'860 teaches the claimed invention.

Contact Information

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Henry Tsai whose telephone number is (571) 272-4176. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 5:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner supervisor, Eddie Chan, can be reached on (571) 272-4162. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to **the TC central telephone number, (571) 272-2100.**

8. In order to reduce pendency and avoid potential delays, Group 2100 is encouraging FAXing of responses to Office actions directly **into the Group at fax number: 703-872-9306.** This practice may be used for filing papers not requiring a fee. It may also be used for filing papers which require a fee by applicants who authorize charges to a PTO deposit account. Please identify the examiner and art unit at the top of your

cover sheet. Papers submitted via FAX into Group 2100 will be promptly forward to the examiner.

HENRY W. H. TSAI
PRIMARY EXAMINER

June 17, 2005